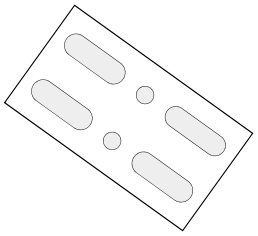
CSP Enhancement Mode Power MOSFET

6208SP Dual N-Channel MOSFET

V_{SSS}	$R_{SS(on)}$TYP	I_S
12V	2.0mΩ@4.5V	12A
	2.1mΩ@3.8V	
	2.3mΩ@3.1V	
	2.8mΩ@2.5V	

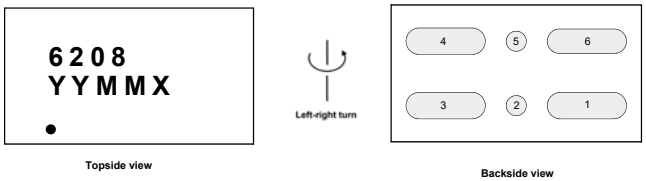
CSPC3117-6



DESCRIPTION

The 6208SP uses advanced trench technology to provide excellent RSS(ON) , low gate charge and operation with gate voltages as low as 2.5V while retaining a 8V $V_{GS(MAX)}$ rating. It is ESD protected. This device is suitable for use as a unidirectional or bi-directional load switch, facilitated by its common-drain configuration.

Marking and pin assignment

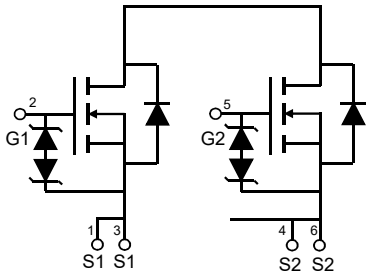


Marking:

1. 6208: Product Code
2. YYMMX: Date Code
3. Solid dot: Pin 1

1,3	Source1
4, 6	Source2
2	Gate1
5	Gate2

Equivalent Circuit



ABSOLUTE MAXIMUM RATINGS (T_a=25℃ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Source to Source Voltage	V_{SSS}	12	V
Gate-Source Voltage	V_{GSS}	±8	V
Source Current(DC)	I_S ①	12	A
Source Current (Pulsed)	I_{SP} ①②	120	A
Total Power Dissipation	P_T ①	2.0	W
Channel Temperature	T_{ch}	150	℃
Storage Temperature Range	T_{STG}	-55 To 150	℃

MOSFET ELECTRICAL CHARACTERISTICS

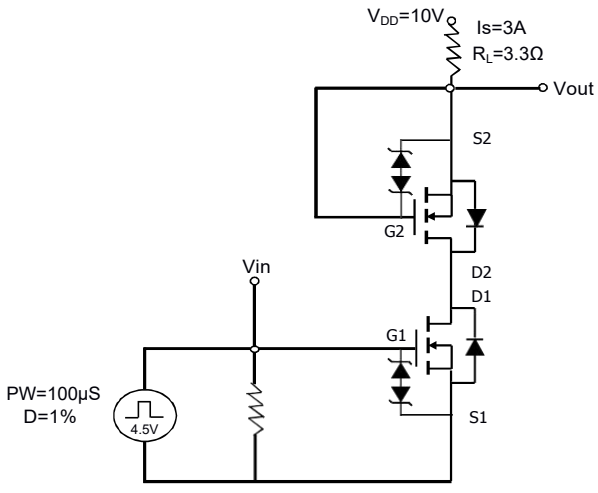
T_a=25 ℃ unless otherwise specified

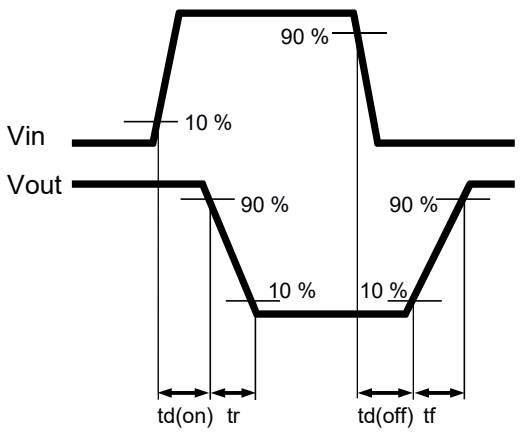
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Static Parameters						
Source to Source Breakdown Voltage	BV_{SSS}	I_S=1mA ,V_{GS}=0V	12			V
Zero-Gate Voltage Source Current	I_{SSS}	V_{SS}=10V,V_{GS}=0V			1.0	μA
Gate to Source Leakage Current	I_{GSS}	V_{SS}=0V,V_{GS}= ±8V			±10	μA
Gate to Source Threshold Voltage	$V_{GS(th)}$	V_{SS}=V_{GS}, I_S=1.41mA	0.4	0.93	1.2	V
Source to Source On-state Resistance	$R_{SS(on)}$	V_{GS}=4.5V,I_S=3A	1.2	2.0	2.8	mΩ
		V_{GS}=3.8V,I_S=3A	1.3	2.1	3.0	mΩ
		V_{GS}=3.1V,I_S=3A	1.4	2.3	3.3	mΩ
		V_{GS}=2.5V,I_S=3A	1.7	2.8	4.0	mΩ
Input Capacitance	Ciss	V_{SS}=10V, V_{GS}=0V,f=1kHz		4262		pF
Output Capacitance	Coss			897		pF
Reverse Transfer Capacitance	Crss			696		pF
Turn-on Delay Time	$t_{d(on)}$ ③	V_{DD}=10V,I_S=3A, V_{GS}=4.5V		1.5		μS
Turn-on Rise Time	t_r ③			4.5		μS
Turn-off Delay Time	$t_{d(off)}$ ③			6.8		μS
Turn-off Fall Time	t_f ③			11.4		μS
Total Gate Charge	Q_g ③	V_{DD}=10V,I_S=6A,V_{GS}=4.5V		49.2		nC
Gate1-source1 charge	Q_{g1s1} ③			10.8		nC
Gate1-source2 charge	Q_{g1s2} ③			25.2		nC
Diode Forward Voltage	$V_{F(S-S)}$	V_{GS}=0V,I_S=3A			1.0	V

Notes: 1.Mounted on FR4 board (25.4mm×25.4mm×t1.0mm) using the minimum recommended pad size (36um Copper).

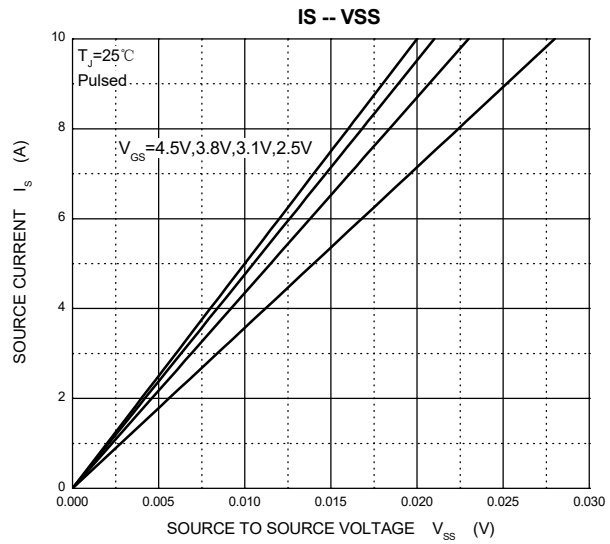
2.t = 10 ms , Duty Cycle = 1 %.

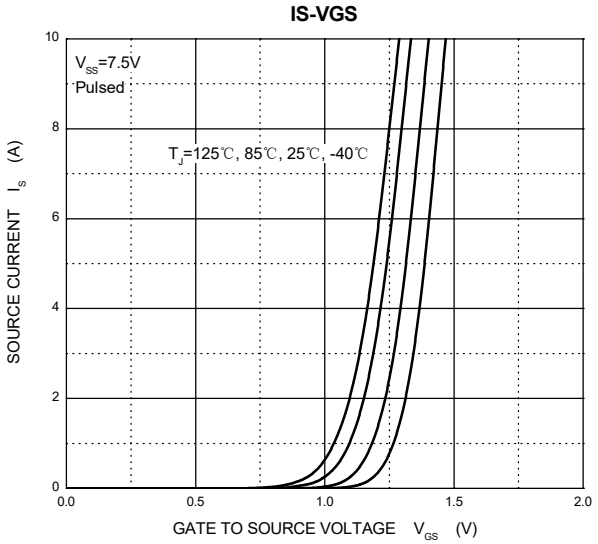
3.When FET1 is measured,G2 and S2 are short-circuited.

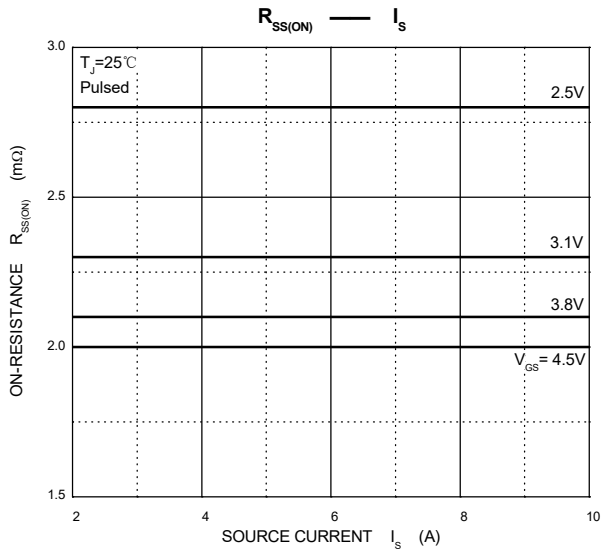


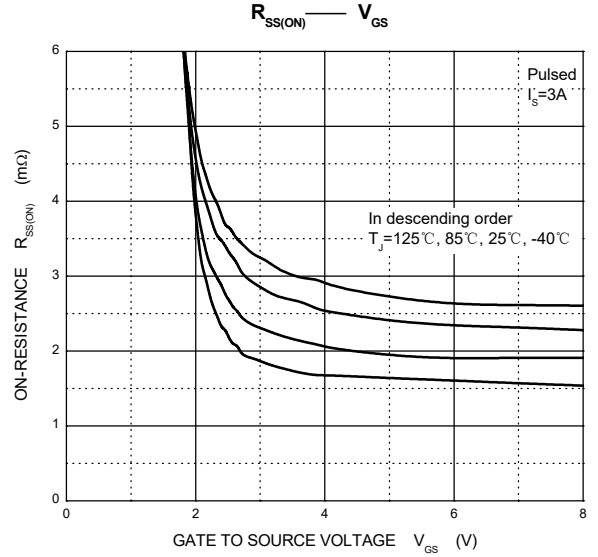


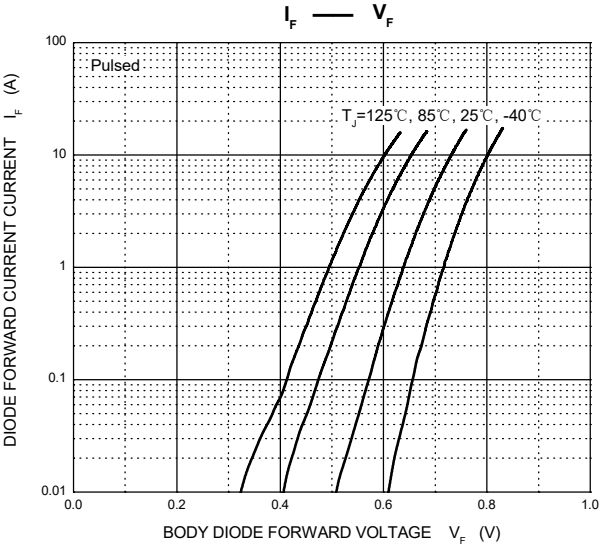
Typical Characteristics

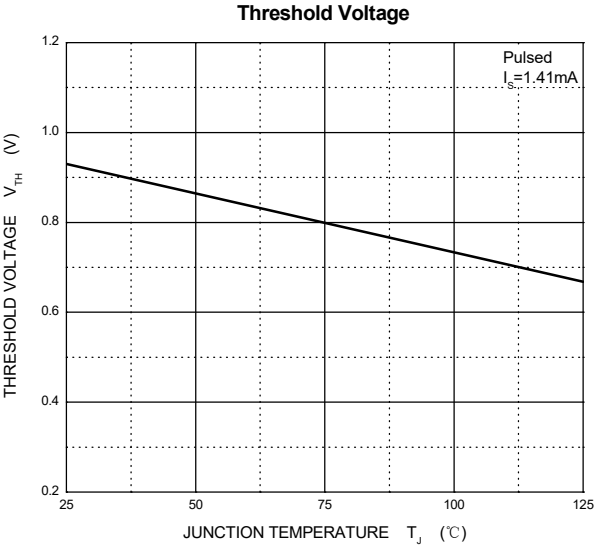






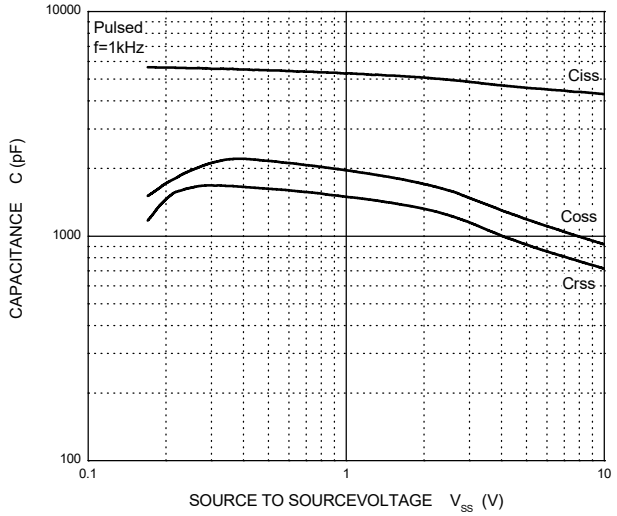




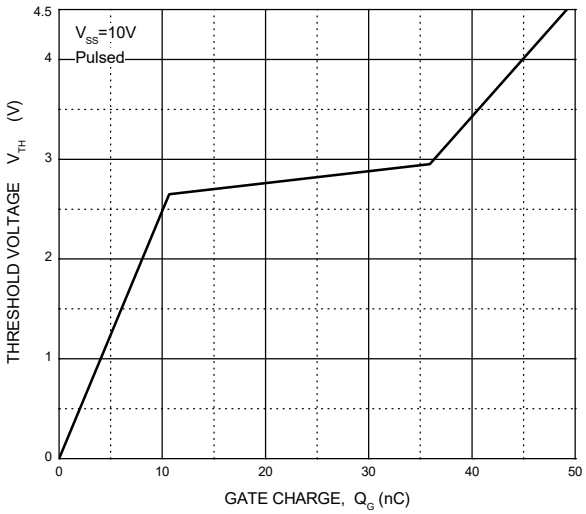


Typical Characteristics

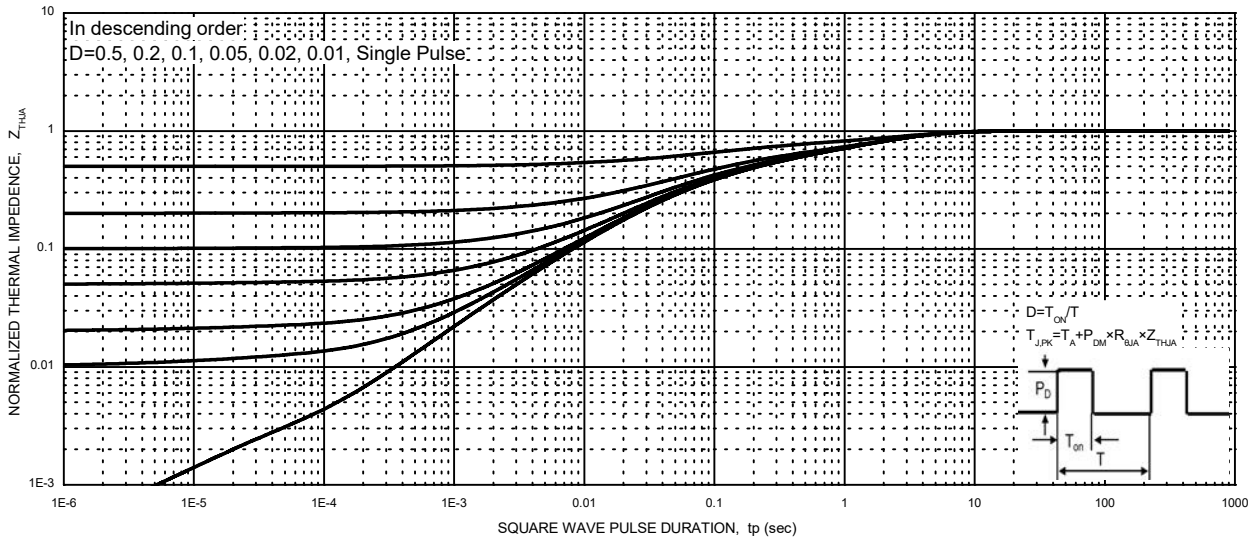
Capacitances



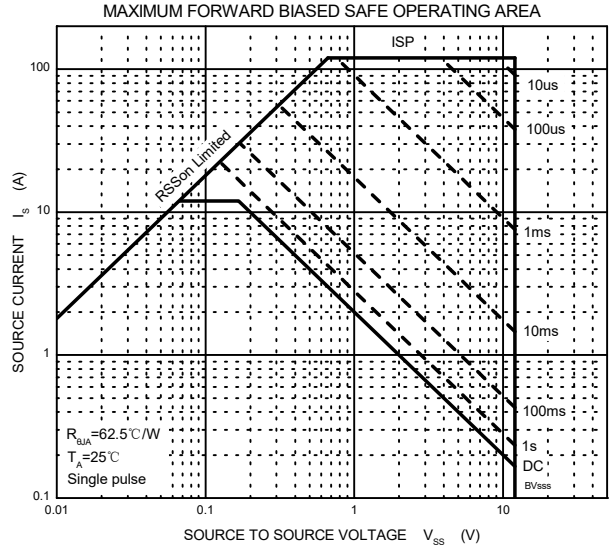
Gate Charge



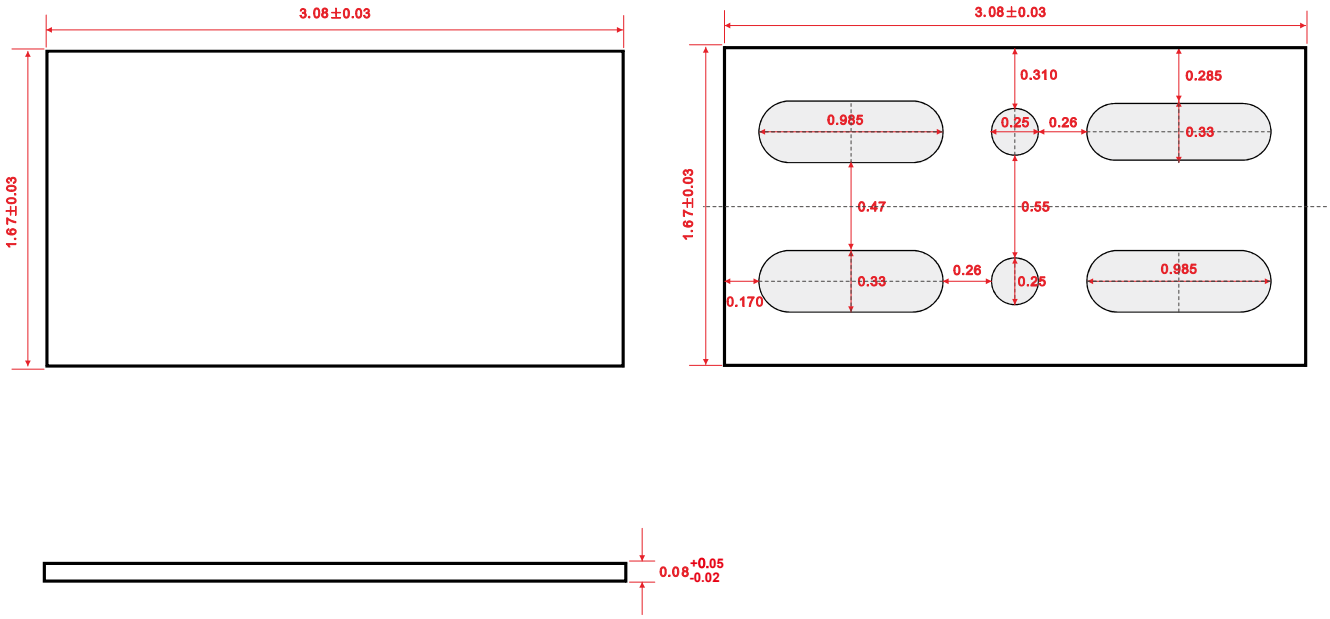
NORMALIZED TRAISIENT THERMAL IMPENDANCE



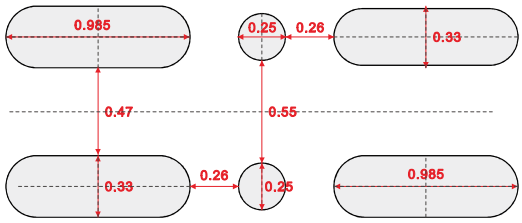
MAXIMUM FORWARD BIASED SAFE OPERATING AREA



CSPC3117-6 Package Outline Dimensions(Unit:mm)



CSPC3117-6 Suggested Pad Layout (Unit:mm)



Note:
1.Controlling dimension:in millimeters.
2.General tolerance:± 0.050mm.
3.The pad layout is for reference purposes only.

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